THAT WHICH IS CLAIMED IS:

1. A large capacity memory device comprising a plurality of memory chips of a certain capacity assembled in a single package and sharing input/output pins, the memories being selectable and singularly enabled one at the time by appropriate external commands coherently with the currently addressed memory location, characterized in that

the device uses only one external enable/disable logic command applied through a single dedicated pin;

each of said memory chips has a number of additional input/output pads equal to $2*n$, if 2^n is the number of memory chips contained in the device, and a dedicated circuit that generates an internal enable/disable command, in function of logic inputs corresponding to the logic states of said additional pads and said external enable/disable command.

2. The memory according to claim 1, characterized in that at least two of said additional input pads are hardwired biased in a coordinated fixed logic states to distinguish each memory chip from the others, the other additional input/output pad or pads are coupled to the pins corresponding to at least one most significant bit of the external address bus applied to the input/output pins of the device.

3. The device according to claim 1, characterized in that said dedicated circuit comprises input buffers functionally coupled to the respective additional pads of

the memory chip and a combinatory logic circuit input with the output signals of said buffers and said external enable/disable command for selecting the memory chip to which the addressed memory position pertains in function of the most significant bit or bits of the external address bus and of the distinguishably of the different memory chips afforded by the configuration of said additional pads fixedly biased in a certain logic state.